Docket No.: R2184.0307/P307
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masaaki Yoshida et al.

Application No.: 10/803,931

Confirmation No.: 6728

Filed: March 19, 2004

Art Unit: 2891

For: SEMICONDUCTOR DEVICE HAVING A PLURALITY OF KINDS OF WELLS AND MANUFACTURING METHOD THEREOF

Examiner: Douglas M. Menz

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the USPTO Official Gazette Notice entitled "Pre-Appeal Brief Conference Pilot Program" published on July 12, 2005, this brief is filed within one month from the mailing date of the Notice of Panel Decision from Pre-Appeal Brief Review mailed May 1, 2007, and is in furtherance of the Notice of Appeal filed by Appellants on March 19, 2007.

The fees required under § 41.20(b)(2) are dealt with in the accompanying Transmittal of Appeal Brief.

This Brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Ricoh Company, Ltd., the assignee of the application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are twenty four claims pending in the application.

B. Current Status of Claims

1. Claims canceled: None
2. Claims withdrawn from consideration but not canceled: 9-24
3. Claims allowed: None
4. Claims rejected: 1-8

C. Claims On Appeal

The claims on appeal are claims 1-8.

IV. STATUS OF AMENDMENTS

Appellants filed a response to the Final Rejection on January 11, 2007, which did not contain any amendments. There have been no claim amendments since the Final Rejection. The

claims enclosed herein in Appendix A incorporate the amendments indicated in the paper filed by Appellants on November 8, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention relates to a semiconductor device (see FIG. 2, reproduced below), in which only one step level difference is formed on the surface of the substrate 10 and in which the maximum level difference between the surface heights of the wells 5, 12, 20 is reduced. Specification, page 8, lines 19-25.

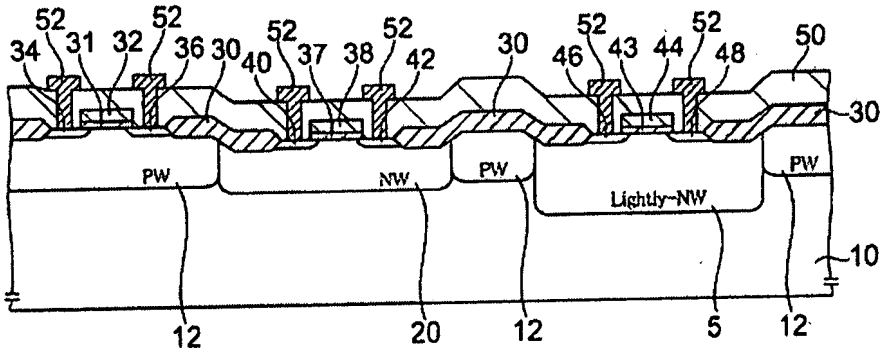
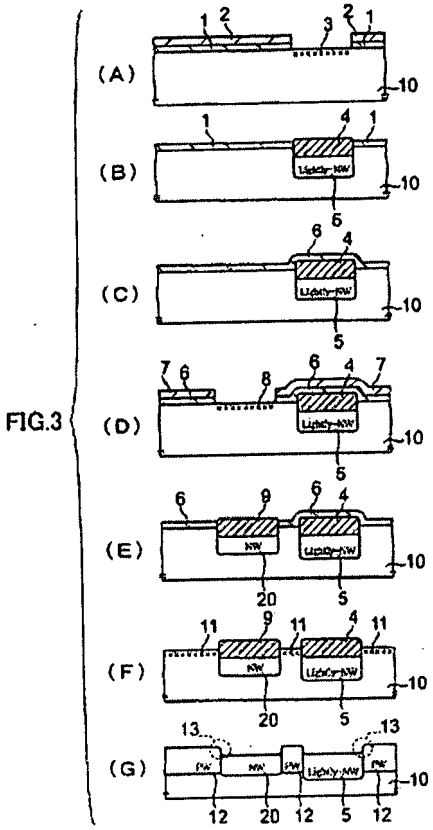


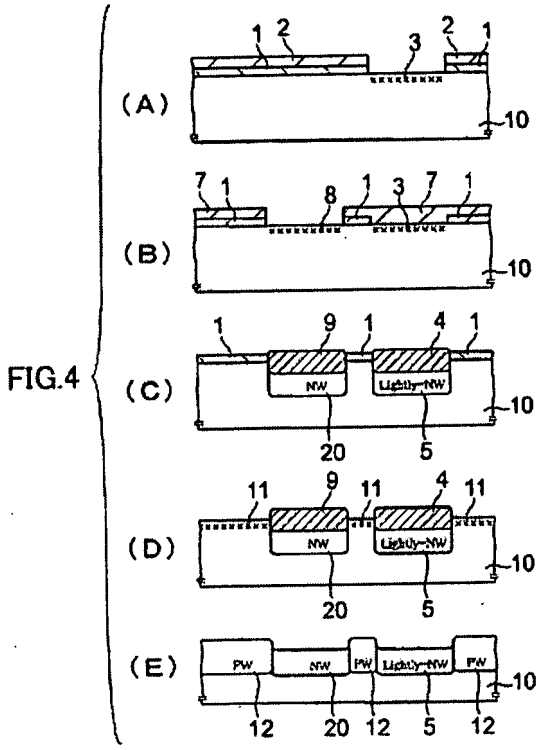
FIG. 2

Referring to FIG. 3, reproduced below (on the next page), the single step level difference 13 may be accomplished by covering the oxide 4 over the first well 5 with a nitride film 6 during growth of the oxide 9 over the second well 20. Specification, page 22, line 12 – page 25, line 1; Figs. 3A-3F. Alternatively, referring to FIG. 4, reproduced below (on the next page), it may be accomplished by growing the oxide layers 4, 9 over each of the first 5 and second 20 wells in the same step. Specification, page 26, line 25 – page 28, line 24; Figs. 4A-4D. After each of these alternatives, the third well 12 is formed, between the previously formed wells 5, 20, with a surface height that is higher than that of the first 5 and second 20 wells. Specification, page 25, lines 2 – 8 and FIG. 3G; Specification, page 28, line 1 – page 29, line 6; and FIG. 4E.

Appellants' FIG. 3



Appellants' FIG. 4



With respect to claim 1, the semiconductor device shown in FIG. 2 has a substrate 10 and at least three kinds of wells 5, 20, 12 formed in and on a top surface of the substrate 10. Specification, page 8, lines 19-25. At least one of the three kinds of wells 12 has a top surface height level higher than the top surface height levels of the other two kinds of wells 5, 20 in relation to the top surface of the substrate 10. Id. The other two kinds of wells 5, 20 also have substantially the same top surface height level as each other and have a different conductivity type than the at least one kind of well 12. Id.

Because the wells 5, 20 have the same top surface height, a single step difference 13 is formed and the maximum level difference between the surface heights is reduced. This single step level difference is important because large level differences (steps) may cause wire-breaking in the wiring of a polysilicon or metal formed over the step. Specification, page 6, lines 21 – 23. Also, if

the level exceeds a focal depth in the photolithography, it becomes difficult to form a device. Specification, page 6, lines 23 – 25.

Although this Brief contains references to the application drawings and specification, the scope of the claims should not be limited thereby. The references are for compliance with § 41.37, and elsewhere to facilitate the Board's understanding of the invention by way of the examples shown and described in the application. The scope of the claims should be determined according to the language of the claims.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The rejection of claims 1-8 under 35 U.S.C. 102(b) as being anticipated by Joy et al. (U.S. Patent No. 4,697,332) ("Joy").

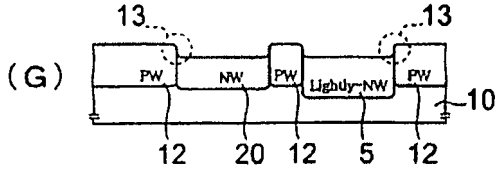
VII. ARGUMENT

A. CLAIMS 1-8 ARE NOT ANTICIPATED BY JOY

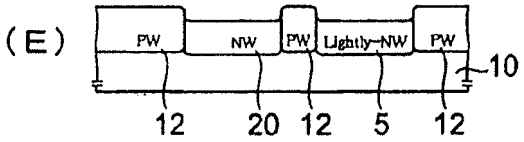
1. Claim 1 is not anticipated by Joy

In order to maintain a rejection under 35 U.S.C. § 102, it is required that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." M.P.E.P. § 2131 (quoting *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987)). In this case, Joy does not disclose each and every element of the claimed invention. Therefore, the rejection of claims 1-8 should be reversed.

Specifically, Joy fails to disclose that at "least one kind of well has a top surface height level higher than the top surface height levels of the other two kinds of wells in relation to the top surface of said substrate, wherein said other two kinds of wells have substantially the same top surface height level as each other," as recited in claim 1. This is an important aspect of the claimed invention, shown for example in FIGS. 3G and 4E, reproduced below (on the next page).



Appellants' FIG. 3G



Appellants' FIG. 4E

The Examiner argues that Joy, Fig. 8g, illustrates a device in which at "least one kind of well has a top surface height level higher than the top surface height levels of the other two kinds of wells . . . wherein said other two kinds of wells have substantially the same top surface height level as each other." Please note, however, the patent drawings of Joy, including Fig. 8g, cannot be used to establish proportions of elements if the specification does not indicate the drawings are to scale. See M.P.E.P. § 2125. Further, while "the description of the article pictured can be relied on, in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art" (M.P.E.P. § 2125, citing *In re Wright*, 569 F.2d 1124 (CCPA 1977)), the description of the figures in Joy makes it clear that Joy does not and cannot form a device as claimed. Joy, col. 8, line 13 – col. 9, line 59.

The method shown and described by Joy in connection with Figs. 8a-8h is essentially the same as the prior art described in Applicants' specification in connection with Appellants' Figs. 1A-1G. The figures are reproduced below (on the next page) and correspond as follows: Joy Fig. 8b corresponds to Appellants' Fig. 1A; Fig. 8d corresponds to Fig. 1B; Fig. 8e corresponds to Fig. 1D; Fig. 8f corresponds to Fig. 1E; Fig. 8g corresponds to Fig. 1F; and Fig. 8h corresponds to Fig. 1G.

Joy, FIG. 8

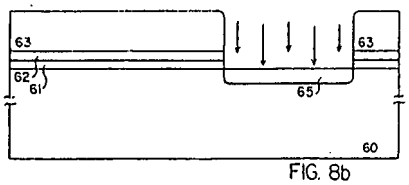


FIG. 8b

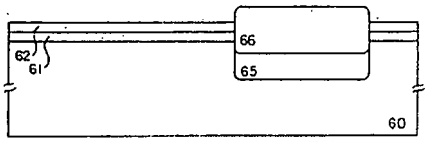


FIG. 8d

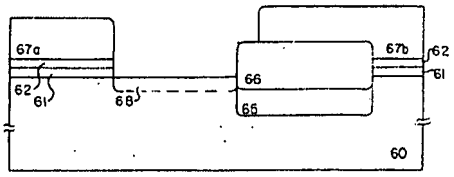


FIG. 8e

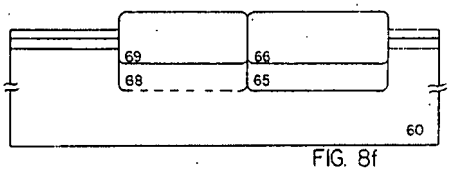


FIG. 8f

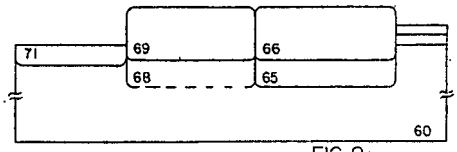


FIG. 8g

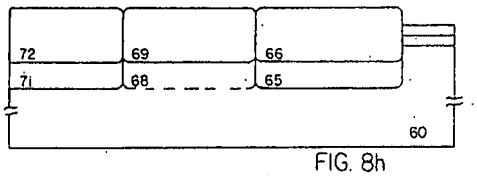
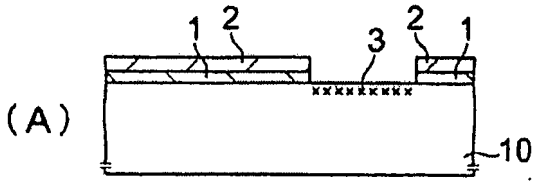
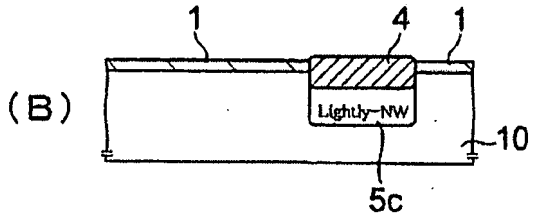
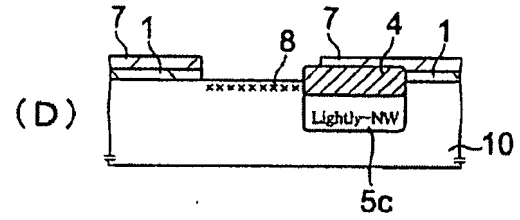


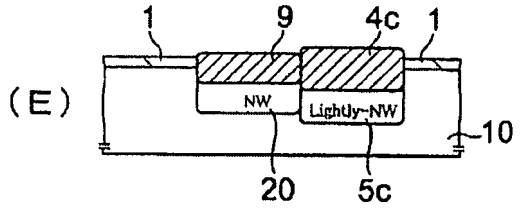
FIG. 8h

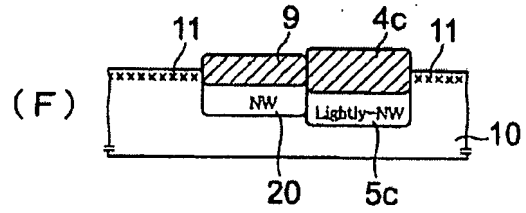
Appellants' FIG. 1

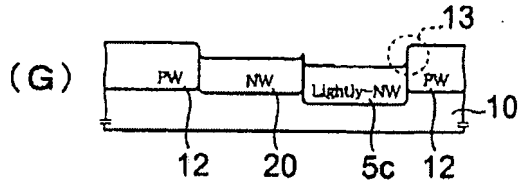












In particular, Joy wells 65 and 68 (Fig. 8g) cannot have the same top surface height (because of the method of formation used) and therefore cannot anticipate the subject matter of claim 1. When oxide 69 is grown over well 68, oxide 66 (of the first formed well 65) is not protected. Therefore, as described both in Joy and in the background of the present application, oxide 66 will thicken during growth of oxide 69; the surface of well 65 will, therefore, become lower than the surface of well 68. Compare Joy, column 9, lines 5-12 to Appellants' Specification, page 5, lines 12-17. The result is substantially the same as that shown in Fig. 1E/1F of the present application. Although the drawings of Joy might seem to show, out of context, that the surfaces of wells 65 and 68 are at the same height, upon reading the specification and applying the knowledge of one skilled in the art, it is apparent that this result is not actually possible, and therefore Joy does not disclose or suggest it. The Examiner has provided no explanation to the contrary.

In light of the above arguments, Appellants respectfully submit that claim 1 is not anticipated by Joy and the 35 U.S.C. § 102(b) rejection should be overturned.

2. Claims 2-8 are not anticipated by Joy

Claims 2-8 depend from claim 1 and are thus allowable along with claim 1. Appellants respectfully submit that claims 2-8 are not anticipated by Joy and the 35 U.S.C. § 102(b) rejection should be overturned.

a. Claim 5 is further allowable over Joy.

Claim 5 further recites "one of said other two kinds of wells has a larger junction depth within said substrate and further includes a triple well in which a well of an opposite conductivity type having a smaller junction depth is formed," illustrated, for example in well 5 of FIG. 7 of the present application. The Examiner asserts that Fig. 8i illustrates a semiconductor device in which "one of said other two kinds of wells has a larger junction depth within said substrate and further includes a triple well in which a well of an opposite conductivity type having a smaller junction depth is formed." Office Action dated October 18, 2006, page 3.

Fig. 8i of Joy, however, does not disclose the limitations of claim 5. Please note that layer 66 over well 65 is an oxide layer 66 (Joy, col. 9, line 60 – col. 10, line 9), and not an additional

well. Therefore, Joy does not disclose "a triple well in which a well of an opposite conductivity type having a smaller junction depth is formed." Appellants respectfully submit that claim 5 is not anticipated by Joy and the 35 U.S.C. § 102(b) rejection should be overturned.

VIII. CONCLUSION

For each of the foregoing reasons, Appellants respectfully submit that the claimed invention is not anticipated by the cited prior art, and reversal of each of the final grounds of rejection is respectfully solicited.

IX. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Appellants on November 8, 2005

Dated: June 1, 2007

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/803,931

1. (Previously presented) A semiconductor device comprising:

a substrate; and

at least three kinds of wells formed in and on a top surface of said substrate,

wherein at least one kind of well has a top surface height level higher than the top surface height levels of the other two kinds of wells in relation to the top surface of said substrate, wherein said other two kinds of wells have substantially the same top surface height level as each other and wherein said other two kinds of wells have a different conductivity type than said at least one kind of well.

2. (Previously presented) The semiconductor device as claimed in claim 1, wherein said other two kinds of wells have the same conductivity type and have different impurity concentrations with relation to each other.

3. (Previously presented) The semiconductor device as claimed in claim 2, wherein at least one kind of well has an impurity concentration that is decreased to a level necessary to form a high-voltage transistor.

4. (Previously presented) The semiconductor device as claimed in claim 1, wherein said other two kinds of wells have different junction depths within said substrate relative to each other.

5. (Previously presented) The semiconductor device as claimed in claim 4, wherein one of said other two kinds of wells has a larger junction depth within said substrate and further includes a triple well in which a well of an opposite conductivity type having a smaller junction depth is formed.

6. (Previously presented) The semiconductor device as claimed in claim 1, wherein said at least one kind of well and said other two kind of wells are of different conductivity types to each other.

7. (Previously presented) The semiconductor device as claimed in claim 1, wherein a MOS transistor is formed by a drain diffusion layer and a source diffusion layer formed in the at least three kinds of wells and a gate electrode formed on areas corresponding to the drain diffusion layer and the source diffusion layer via a gate insulating film.

8. (Previously presented) The semiconductor device as claimed in claim 5, wherein MOS transistors are formed by drain diffusion layers and source diffusion layers formed in the at least three kinds of wells and gate electrodes formed on areas corresponding to the drain diffusion layers and the source diffusion layers via a gate insulating film, and wherein one of the MOS transistors formed on the triple well is one of a MOS transistor constituting a power supply circuit, a MOS transistor constituting a circuit sensitive to a substrate noise and a MOS transistor constituting a circuit generating a noise.

9. (Withdrawn) A manufacturing method of a semiconductor device having more than three kinds of wells in a single substrate, comprising the steps of:

(A) forming a first silicon nitride film on said substrate;

(B) forming a first resist pattern by a photolithography so as to define a first well area, removing a part of said first silicon nitride film corresponding to an opening of said first resist pattern by etching, introducing first impurity ions into said first well area of said substrate by ion implantation so as to form said first well area, and removing said first resist pattern;

(C) applying a heat treatment to said substrate within an oxidizing atmosphere so as to form a first thermal oxide film on an area of a surface of said substrate that is not covered by said first silicon nitride film and simultaneously diffuse the first impurity ions introduced into said substrate to form the first well;

(D) removing said first silicon nitride film, forming a second silicon nitride film on said substrate including said first thermal oxide film, forming a second resist pattern on said second

silicon nitride film by a photolithography so as to form a second well area, removing a part of said second silicon nitride film corresponding to an opening of said second resist pattern by etching so as to define said second well area, introducing second impurity ions into said second well area of said substrate by ion implantation so as to form the second well, and removing said second resist pattern;

(E) applying a heat treatment to said substrate within an oxidizing atmosphere the same as said oxidizing atmosphere in the step (C) so as to form a second thermal oxide film on an area of a surface of said substrate that is not covered by said second silicon nitride film and simultaneously diffuse the second impurity ions introduced into said substrate to form the second well;

(F) removing said second silicon nitride film, and introducing third impurity ions into said substrate by using said first and second thermal oxide films as masks so as to form a third well area in a self-alignment manner; and

(G) applying a heat treatment to said substrate in a non-oxidizing atmosphere so as to diffuse the third impurity ions to form the third well.

10. (Withdrawn) The manufacturing method as claimed in claim 9, wherein the processes of steps (D) and (E) are repeated for a plurality of times while changing at least one of a kind of said second impurity ions, an amount of said second impurity ions to be introduced and an implantation condition of said second impurity ions.

11. (Withdrawn) A manufacturing method of a semiconductor device having more than three kinds of wells in a single substrate, comprising the steps of:

(A) forming a silicon nitride film on said substrate;

(B) forming a first resist pattern by a photolithography to define a first well area, removing a part of said silicon nitride film corresponding to an opening of said first resist pattern by etching, introducing first impurity ions into said first well area of said substrate by ion implantation so as to form said first well area, and removing said first resist pattern;

(C) forming a second resist pattern by a photolithography so as to form a second well area, removing a part of said silicon nitride film corresponding to an opening of said second resist pattern by etching so as to define said second well area, introducing second impurity ions into said

second well area of said substrate by ion implantation so as to form the second well, and removing said second resist pattern;

(D) applying a heat treatment to said substrate within an oxidizing atmosphere so as to form a thermal oxide film on an area of a surface of said substrate that is not covered by said silicon nitride film and simultaneously diffuse the first and second impurity ions introduced into said substrate to form the first and second wells;

(E) removing said silicon nitride film, and introducing third impurity ions into said substrate by using said thermal oxide film as a mask so as to form a third well area in a self-alignment manner; and

(F) applying a heat treatment to said substrate in a non-oxidizing atmosphere so as to diffuse the third impurity ions to form the third well.

12. (Withdrawn) The manufacturing method as claimed in claim 11, wherein the step (B) includes a step of applying a heat treatment in a non-oxidizing atmosphere before proceeding to a subsequent ion implantation process.

13. (Withdrawn) The manufacturing method as claimed in claim 12, wherein the step (B) includes a step of applying a heat treatment to said substrate in an oxidizing atmosphere so as to form a protective oxide film on the surface of said substrate before applying the heat treatment in said non-oxidizing atmosphere.

14. (Withdrawn) The manufacturing method as claimed in claim 13, wherein said protective oxide film has a thickness in a range of 10 nm to 50 nm.

15. (Withdrawn) The manufacturing method as claimed in claim 11, wherein the process of step (B) is repeated for a plurality of times while changing at least one of a kind of said first impurity ions, an amount of said first impurity ions to be introduced and an implantation condition of said first impurity ions.

16. (Withdrawn) The manufacturing method as claimed in claim 11, further comprising a step of applying a heat treatment to said substrate in a non-oxidizing atmosphere after repeating the process of step (B) and before proceeding to a subsequent ion implantation process.

17. (Withdrawn) The manufacturing method as claimed in claim 16, further comprising a step of applying a heat treatment to said substrate in an oxidizing atmosphere so as to form a protective oxide film on the surface of said substrate before applying the heat treatment in said non-oxidizing atmosphere.

18. (Withdrawn) The manufacturing method as claimed in claim 17, wherein said protective oxide film has a thickness in a range of 10 nm to 50 nm.

19. (Withdrawn) The manufacturing method as claimed in claim 9, wherein a deeper well is formed earlier.

20. (Withdrawn) The manufacturing method as claimed in claim 9, further comprising a step of forming a third resist pattern within a specific well by a photolithography so as to define a triple well before applying the final heat treatment in said non-oxidizing atmosphere, introducing fourth impurity ions of a conductivity type opposite to said specific well into said substrate under a condition in which a depth of said triple well becomes shallower than said specific well, and removing said third resist pattern.

21. (Withdrawn) The manufacturing method as claimed in claim 9, wherein the final heat treatment in said non-oxidizing atmosphere is omitted so that the third impurity ions are diffused by a heat treatment applied when performing a field oxidation for element isolation.

22. (Withdrawn) The manufacturing method as claimed in claim 11, wherein a deeper well is formed earlier.

23. (Withdrawn) The manufacturing method as claimed in claim 11, further comprising a step of forming a third resist pattern within a specific well by a photolithography so as to define a triple well before applying the final heat treatment in said non-oxidizing atmosphere, introducing

fourth impurity ions of a conductivity type opposite to said specific well into said substrate under a condition in which a depth of said triple well becomes shallower than said specific well, and removing said third resist pattern.

24. (Withdrawn) The manufacturing method as claimed in claim 11, wherein the final heat treatment in said non-oxidizing atmosphere is omitted so that the third impurity ions are diffused by a heat treatment applied when performing a field oxidation for element isolation.

APPENDIX B

A copy of evidence entered by or relied upon by the Examiner that is relevant to this appeal is attached hereto. Exhibit 1 was first entered by the Examiner in the Office Action mailed February 3, 2006.

Exhibit 1: U.S. Patent No. 4,697,332 to Joy et al.